Amend claim 10 as follows:

10. (Twice Amended) A transistor structure which comprises:

a region of semiconductor material having a gate dielectric thereover;

a polysilicon gate disposed over said gate dielectric having a top, a bottom and sidewalls;

a silicide layer disposed on said top and sidewalls of said polysilicon gate; and

source/drain regions in said region of semiconductor material spaced apart from each other, said source/drain regions [and] each disposed adjacent to and aligned with said silicide layer disposed on said sidewalls.

REMARKS

Claims 8 to 10 have been amended. Claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 remain active in this application.

Claim 10 was rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In this regard, the Examiner questions the recitation of source/drain regions each disposed adjacent to and aligned with the silicide layer disposed on the sidewalls. The rejection is respectfully traversed. Reference is invited to the specification at page 8, lines 7 to 11 wherein it is stated "[a]fter deposition, the source/drain areas receive their final doping, which is implanted (step 145) through the layer of metal to form regions 80. It is noted that the conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant.". It follows that the source/drain regions are aligned with the silicide layer and this fact is in the disclosure as originally filed.

Claims 8 and 9 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The rejection is respectfully traversed. Claims 8 and 9 set forth "a patterned gate" in line 3 of each claim, this providing the required antecedent basis in that claim.

Claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (U.S. 5,841,174) in view of Watabe et al.(4,727,038) or Tada (Japan 4-42938).

Claims 8 and 9 require, among other features, a lateral growth on the gate dielectric at the corners of the gate, but not under central regions of the gate, the thickness of the gate dielectric continually increasing at the interface of the bottom surface and the sidewalls sidewalls of the gate in a direction from the bottom surface toward and along the sidewalls. This provides increased gate conductivity, additional control over gate corner profiles, additional control over gate electric fields, additional control over silicided gate structures and additiona control over the line-to-space ratio of the gate pattern, while using conventional processing techniques. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references taken alone or in the combination as claimed.

Claim 10 requires, among other features, a silicide layer disposed on the top and sidewalls of the polysilicon gate and source/drain regions in the region of semiconductor material spaced apart from each other and each disposed adjacent to and aligned with the silicide layer disposed on the sidewalls. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references taken alone or in the combination as claimed.

Claims 12, 14, 16, 18, 20, 22, 24, 26 and 27 depend from claim 10 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 10.

Claim 12 further limits claim 10 by requiring that the silicide layer be titanium silicide. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references in the combination as claimed.

Claims 14 and 16 further limit claims 10 and 12 by requiring a lightly doped source/drain extension of each of the source/drain regions extending under the polysilicon gate. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references in the combination as claimed.

Claims 18, 20, 22 and 24 further limit claims 10, 12, 14 and 16 by requiring a dielectric extending from the gate dielectric of increased thickness relative to the gate dielectric and disposed under the silicide layer. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

Claim 26 further limits claim 10 by requiring that the silicide layer extend to the gate dielectric. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

Claim 27 further limits claim 18 by requiring that the silicide layer extend to said dielectric of increased thickness. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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